IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
TYLER DIVISION

U.S. ETHERNET INNOVATIONS, LLC, **Plaintiff,** **v.** **TEXAS INSTRUMENTS INCORPORATED,** **Defendant.**	 **6:11-cv-491-MHS-JDL** **PATENT CASE**
U.S. ETHERNET INNOVATIONS, LLC, **Plaintiff,** **v.** **RICOH AMERICAS CORPORATION,** **Defendant.**	 **6:12-cv-235-MHS-JDL** **CONSOLIDATED LEAD CASE** **PATENT CASE**
U.S. ETHERNET INNOVATIONS, LLC, **Plaintiff,** **v.** **TRENDNET, INC.,** **Defendant.**	 **6:12-cv-236-MHS-JDL** **CONSOLIDATED CASE** **PATENT CASE**
U.S. ETHERNET INNOVATIONS, LLC, **Plaintiff,** **v.** **XEROX CORPORATION,** **Defendant.**	 **6:12-cv-237-MHS-JDL** **CONSOLIDATED CASE** **PATENT CASE**

U.S. ETHERNET INNOVATIONS, LLC, **Plaintiff,** **v.** **KONICA MINOLTA BUSINESS SOLUTIONS U.S.A., INC., et al.,** **Defendants.**	 **6:12-cv-329-MHS-JDL** **CONSOLIDATED CASE** **PATENT CASE**
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DEFENDANTS' *MARKMAN* BRIEF

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I. INTRODUCTION

Defendants[1] hereby file this brief on claim construction issues with regard to certain claim terms of U.S. Patent Nos. 5,434,872 ("'872 Patent"), 5,732,094 ("'094 Patent"), 5,530,874 ("'874 Patent"), 5,307,459 ("'459 Patent"), and 5,299,313 ("'313 Patent").[2] Defendants' proposed constructions are consistent with the intrinsic evidence and, accordingly, correct.

The asserted patents relate to alleged minor improvements to network adapters used in the early 1990s to connect computers to Ethernet networks.[3] In other words, the patents are directed to problems allegedly prevalent twenty years ago, when computers were thousands of times slower than today, and networks were local instead of global. Moreover, even the so-called "improvements" claimed in the patents-in-suit were non-novel and obvious in light of the prior art, as shown in Defendants' invalidity contentions. Faced with the challenge of trying to apply obsolete patents to the Defendants' advanced technologies against a backdrop of invaliding prior art, Plaintiff U.S. Ethernet Innovations ("USEI") tries strenuously to contort the contours of the patent claims – ignoring the intrinsic evidence, trial testimony of the lead inventor on the asserted patents, and its own expert witness in the process. These attempts should fail, and the Court should reject Plaintiff's constructions in their entirety.

II. CLAIM TERMS IN DISPUTE

A. "network interface device," "network interface adapter," "network

[1] Collectively, "Defendants" means and includes Texas Instruments, Inc., Ricoh Americas Corporation, TRENDnet, Inc., Xerox Corporation, Konica Minolta Business Solutions U.S.A., Inc., Freescale Semiconductor, Inc., Digi International Inc., NetSilicon, Inc., Epson America, Inc., Cirrus Logic, Inc., Yamaha Corporation of America, Control4 Corporation, NETGEAR, Inc., Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Telecommunications America, LLC, Samsung Austin Semiconductor, LLC, Oki Data Americas, Inc., and STMicroelectronics, Inc. Plaintiffs have not yet served Defendant STMicroelectronics N.V. ("STNV"). STNV has not yet filed an answer or otherwise appeared in this case, and does not participate in this filing.

[2] The asserted patents are attached hereto as Exhibits A-1 through A-5, respectively.

[3] Defendants' Technical Tutorial (filed February 20, 2013) provides a more detailed explanation of the patents-in-suit.

adapter," "network adapter device"[4]

USEI's Position	Defendants' Position
plain and ordinary meaning; alternatively: "device that interfaces between a communications network and a host system"	"a connectable device that enables communication between a computer system and a network"

As an initial matter, the Court has ordered that Defendants may brief why these four similar terms require the same construction. *See* Dkt. 166, Civ. A. No. 6:12-cv-235-MHS. Across the asserted patents, the four terms are used interchangeably. For instance, the '874 Patent's claims use three of these terms interchangeably. *Id.* at 6–7. Additionally, the '094 Patent and '872 Patent share the same specification, but use different terms in their claims ("network interface device" and "network interface adapter," respectively) to refer to the same device. *Id.* The related '459 Patent, which was filed the same day, uses "network adapter" in its claims. *Id.* Finally, the specifications of the four patents describe their alleged invention in terms of a "network adapter," "network interface adapter," and "network interface controller," all of which apparently refer to the same device. *Id.* Even USEI agrees that, to the extent the Court construes all four terms, the same construction should apply. Plf. Br. at 6, n.4.

The first dispute between the parties over the term "network adapter" and its related terms is whether any construction is needed at all.[5] It is well-settled that when the meaning of a claim term is disputed, the court must construe the term as a matter of law. *O2 Micro Intern. Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1360–62 (Fed. Cir. 2008). Moreover,

[4] These claim terms appear in Claims 1 and 39 of the '094 Patent (Ex. A-2), Claim 21 of the '872 Patent (Ex. A-1), Claims 22, 26, 27, 28, 31, 32, 34, 36, 39, 44, 46, 47, 49, 50 of the '459 Patent (Ex. A-4), and Claims 21, 23, 29, 30 of the '874 Patent (Ex. A-3).

[5] Defendants will use the term "network adapter," the term appearing most commonly in the asserted claims, in the following discussion to refer to all four terms.

when the term at issue is a term of art, like "network adapter," rather than a common English word, claim construction is highly appropriate. *Multiform Desiccants, Inc. v. Medzam, Ltd.*, 133 F.3d 1473, 1476 (Fed. Cir. 1998).

The substantive dispute is whether "network adapter" refers to a device that must be "connectable." As explained below, all of the intrinsic evidence – and all available extrinsic evidence, including the testimony of the lead inventor and USEI's own expert witness – points to a single conclusion: a person of ordinary skill in the art at the time of the invention[6] would have understood "network adapter" to refer to a "connectable" device. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). USEI's suggestion to the contrary is incorrect.

The specifications of the patents-in-suit support the conclusion that a "network adapter" must be "connectable." Consistent with the state of the art in 1992, *every disclosed embodiment* of the "network adapter" possesses the fundamental characteristic of being "connectable." More specifically, the network adapters in the specification are cards or boards that are plugged into, *i.e.*, connectable with, the bus of a host system. Ex. A-5, '313 Patent, 1:25 (card); Ex. A-1, '872 Patent, 6:10–12 (board), 8:58 (onboard), 29:27 (onboard). Indeed, several figures show that the network adapter connects to the host system via an EISA bus, which necessarily means that the network adapter is a separate card or board that is connectable. Ex. A-1, '872 Patent, 4:2–3, 4:26–29, 5:30–31, Figs. 1, 2, 3; Ex. A-3, '874 Patent, 4:52–56, Figs. 1, 2.

The prosecution history also supports Defendants' position. While prosecuting the '872 Patent, the inventors referred to their invention as a "card" multiple times. *See* Ex. A-7, '872 Pros. Hist., March 2, 1994 Decl. at p. 2 ¶ 1 (card), ¶ 2 (card), Exhibit 1 at p. 2 (adapter card), p. 3

[6] The effective filing dates of the asserted patents are 1992 or early 1993. USEI asserted an even earlier date of invention – 1990 – in its Infringement Contentions. *See e.g.,* Ex. A-6, Plf. P.R. 3-1 Disclosures to STMicroelectronics Inc. at 7–8.

(card). Similarly, during prosecution of the '094 Patent, the Applicants referred to their device as an "adapter card." A-8, '094 Pros. Hist., Applicant Remarks of April 7, 1997 at p. 5, ¶ 4. A card is a separate device that is connected to – and thus connectable with – the host.

Defendants' construction also finds ample support in the extrinsic evidence. Brian Petersen, the first named inventor on four of the asserted patents, testified in a prior litigation that "network adapters . . . are cards that you plug into a computer to provide Ethernet connectivity for computers of the era that did not have those as standard features." A-9, Trial Tr. at 91:14–18, *3Com Litigation* (N.D. Cal. May 9, 2003). Mr. Petersen further equated "network adapters" with "network cards." *Id.* at 91:19–20.

Similarly, USEI's own expert witness, Dr. Mitzenmacher, has described the network adapter as a separate network interface controller (NIC) card, testifying that "[t]he NIC card is attached to the computer. It's coupled to the host system. ***The NIC card isn't part of the host system.*** . . . ***[Y]ou plug it into the slot***. We referred to the host system in the patent as being the computer and the card as being the separate object that is being interfaced with the host system." *Id.* at 417:3–10 (emphasis added). Dr. Mitzenmacher has also testified that the alleged point of novelty of the '313 Patent was that the "buffer memory . . . [is] located on [an] **additional device** which exists outside the traditional host memory space, that is [the buffer memory] is under the control of this **additional device**." Ex. A-10, Deposition Tr. at 21:5–22:6, *Acer Litigation* (N.D. Cal. Oct. 9, 2009) (emphasis added).[7]

Technical dictionaries from the early 1990s agree that a "network adapter" is a

[7] In addition, on numerous occasions, Mr. Petersen and Dr. Mitzenmacher have simply referred to the network adapter as a "card," reflecting the common and deeply ingrained understanding of the term in the art. *See, e.g.,* Ex. A-9, Trial Testimony of Brian Petersen at 91:14–20; 93:5–22; 94:1–8; 95:22–96:9; 102:3–18, *3Com Litigation* (N.D. Cal. May 9, 2003); Ex. A-9, Trial Testimony of Dr. Mitzenmacher at 214:12–23; 417:3–10, *3Com Litigation* (N.D. Cal. May 9, 2003); Ex. A-10, Deposition of Dr. Mitzenmacher at 21:5–22:16; 83:3–18; 84:23–85:6; 105:7–19; 106:6–25; 108:16–109:1; 178:5–21; 199:1–17; 210:9–16, *Acer Litigation* (N.D. Cal. Oct. 9, 2009).

connectable device, defining it as a "[p]rinted circuit board that plugs into a workstation or server and controls the exchange of data over a network"; "[a]n expansion card or other device used to connect a computer to a local area network"; or "[a]n adapter that enables one to hook a network cable directly to a microcomputer."[4] USEI, however, seeks to impermissibly broaden the meaning of "network adapter" beyond its plain meaning in the early 1990s by reading out the common understanding that a network adapter is "connectable." USEI misinterprets its own specification in arguing that "the patent clearly contemplated an embodiment in which the network controller [*i.e.*, network adapter] is implemented in a chip, such as an integrated circuit." Plf. Br. at 7. The specification does not say that the network adapter is *itself* an integrated circuit; rather, the network adapter "**includes** a network interface processor 14, implemented in one preferred system as an application specific integrated circuit." Ex. A-3, '874 Patent, 5:47–50 (emphasis added). In other words, the network adapter is a separate card that includes separate integrated circuits, such as the "network interface processor 14," RAM 15, and "encode/decode chip 19," that implement different aspects of the network adapter. *See id.* at 5:45–58, 6:18–27, Fig. 3.

Further, even if the patent specification *did* say that the entire network adapter could itself be an integrated circuit, that would still support the conclusion that the network adapter is connectable. An integrated circuit is typically packaged into a self-contained housing with pins for electrical contact, which in turn can be connected to a host through an EISA bus – just as with a card or board. *See id.* at 5:53–55, Fig. 3.

Unlike Defendants' proposal, USEI's proposed construction lacks support in either the intrinsic or extrinsic evidence. First, the specification does not disclose any embodiments in

[4] Ex. A-11, The Computer Glossary (6th ed. 1993); Ex. A-12, The Microsoft Press Computer Dictionary (2d ed. 1994); Ex A-13, Webster's New World Dictionary of Computer Terms (4th ed. 1992).

which the network adapter is an integrated part of the host, as USEI's proposal would allow. Second, the prosecution history does not describe a single embodiment reflecting USEI's broader proposal. Third, USEI has not submitted any relevant extrinsic evidence. Indeed, the only purported sources of extrinsic evidence cited by USEI are technical dictionaries from ten years or more after the time of the alleged invention. Ex. A-14, Plf. 4-3, Exh. A at 4. It is well-established that the relevant time period for determining claim meaning is the time of the invention – not a decade later. *Kopykake Enterprises, Inc. v. Lucks Co.*, 264 F.3d 1377, 1383 (Fed. Cir. 2001). Finally, the repeated testimony of the lead inventor and USEI's own expert supports the construction proffered by defendants, not USEI.

B. "indication value," "first indication signal," "first masked signal," "masked indication signal"[8]

USEI's Position	Defendants' Position
plain and ordinary meaning; alternatively: "value indicating one or more asynchronous events"	"signal representing an event that is output from one level of masking and is input into a second level of masking, and that may or may not trigger generation of a corresponding interrupt signal"

As a threshold matter, Defendants request that the Court apply a single construction to "indication value," "first indication signal," "first masked signal," and "masked indication signal." The "indication value" of Claim 1 is synonymous with "first indication signal" of Claim 21, "first masked signal" of Claim 23, and "masked indication signal" of Claim 29 because they all have the same sequential signal structure. In all cases, the signal in question is output from one level of masking and input to a second level of masking.[9] The synonymous terms of Claims

[8] These terms appear in Claims 1, 2, 4, 7, 21, 23, 25, 26, 29, 30 of the '874 Patent. Defendants' brief addresses why these four similar terms require the same construction. *See* Dkt. 166, Civ. A. No. 6:12-cv-235-MHS.

[9] Ex. A-3, '874 Patent, Claim 1 ("a first mask logic . . . to output an *indication value*; . . . a second mask logic . . . for receiving the *indication value*"); Claim 21 ("selectively masking … to output a ***first indication signal;*** … selectively masking at least a portion of the ***first indication signal***"); Claim 23 ("selectively masking … to output a set of ***first masked signals;*** … selectively masking at least a subset of the ***first masked signals***"); Claim

21, 23, and 29 are not defined or even used in the '874 specification. They were not included in the originally-filed claims, but were added during the prosecution of the '874 Patent.[10] Importantly, both the patent examiner and applicants concluded that the analysis of Claim 1 was to be applied to the new claims with the synonymous terms.[11]

The '874 Patent discloses a network adapter with two sequentially arranged masks – an indication signal mask and an interrupt signal mask. Ex. A-3, '874 Patent, Abstract and Title. By using two levels of masking, an indication signal can be selectively disabled by either mask so that it does not result in an interrupt signal to the host. *Id.* at Abstract, 2:40–54. According to Claim 1, the indication signal is input and the interrupt signal is output, but in between input and output the signals are referred to as an "indication value" or "interrupt value."

Fig. 12 of the'874 Patent shows the progression of signals.

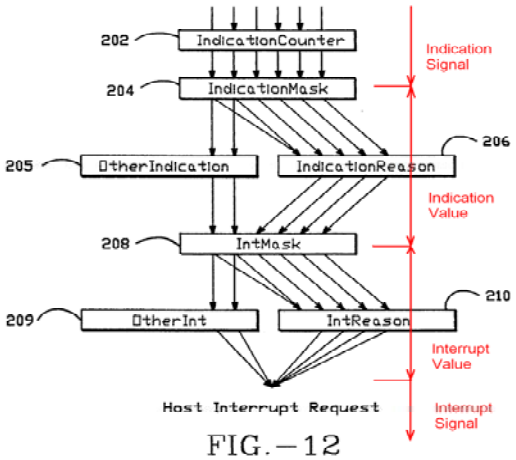

FIG.—12

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29 ("an indication signal mask device … having a plurality of ***masked indication signal*** outputs; … an interrupt signal mask device coupled to said plurality of ***masked indication signal*** outputs") (emphasis added)

[10] A-15, '874 Pros. Hist., February 9, 1995 Response at 11–12 (new Claims 22 and 25 (corresponding to issued Claims 21 and 23)); A-16, '874 Pros. Hist., August 18, 1995 Response at 10–12 (new Claim 31 (corresponding to issued Claim 29)).

[11] A-15, '874 Pros. Hist., February 9, 1995 Response at 19 ("In light of Applicants' discussion above with respect to the patentability of amended Claims 1–21, new method Claims 22–30, which cover multiple levels of mask logic and memory locations for managing indication signals to present an interrupt signal to a host, are allowable."); A-17, '874 Pros. Hist., May 19, 1995 Office Action at 6 ("For claims 22–30, due to the similarity between the claims, the teachings of the claims 1–7 and 10–13, 17 are similarly applied."); A-16, '874 Pros. Hist., August 18, 1995 Response at 14 ("The inventions of Claims 10–13, 21–22 and 24–32, are allowable over the cited references for reasons similar to those for allowance of Claim 1.").

Id. at Fig. 12 (modified in red). The *indication signal* is input to a first mask – Indication Mask 204.[12] *Id.* at 26:53–30:36, 31:29–57. The Indication Mask 204 is a register that contains bits provided by the host computer that disable the *indication signal* or allow it to pass through. The output of the first mask is called an *indication value*, and is stored in the Other Indication and Indication Reason registers 205 and 206 where it can be read by the host system. The *indication value* is input to a second mask – Int Mask 208 – which is also a register that contains bits that disable the indication value or allow it to pass through. The output of the second mask, called an *interrupt value*, is stored in the Other Int and Int Reason registers 209 and 210. From there, the *interrupt value* is used to generate an *interrupt signal*.

The '874 specification and Claim 1 support Defendants' construction of "indication value." Claim 1 distinguishes among four signals – the indication signal, indication value, interrupt value and interrupt signal – depending upon where they are relative to the masks and interrupt means. "Indication value" is the signal that exists between the two masks because it is output from the first mask ("a first mask logic … to output an indication value") and input to the second mask ("a second mask logic … for receiving the indication value"). *Id.* at Claim 1. Because the indication value is subject to the downstream second mask and interrupt means, it may or may not trigger the generation of a corresponding interrupt signal. Furthermore, the indication value is a signal representing an event. *Id.* at 3:1.

The prosecution history of the '874 Patent also supports Defendants' proposed construction. In the first office action, the patent examiner rejected Claim 1 as indefinite. A-18, '874 Pros. Hist., September 20, 1994, Office Action at 2. In response, the Applicants amended Claim 1 to require the first mask logic "to output an indication value" and the second mask logic

[12] The Indication Counter 202 is not at issue in the asserted claims, so it is not relevant here.

for "receiving the indication value." Ex. A-15, February 9, 1995, Response at 2. In a later response, the Applicants reiterated that Claim 1 "requires that the second mask logic be coupled to receive the indication value." Ex. A-16, August 18, 1995, Response at 13.

USEI argues for "plain and ordinary meaning," but fails to explain what "indication value" means in plain English. The term "indication value" is neither a commonplace term, nor does USEI argue, as it cannot, that this is a term used in the art. Rather, it has a specific meaning in the context of the '874 Patent. As such, construction is required to assist the factfinder. Accordingly, the Court should provide a meaningful construction for this disputed term. *See also O2 Micro Intern.*, 521 F.3d at 1360–62 (claim must be construed where disputed).

USEI's alternative construction – "value indicating one or more asynchronous events" – is too general because all four sequential signals – indication signal, indication value, interrupt value, and interrupt signal – represent asynchronous events.[13] Since USEI's construction would not distinguish among the four signals, it will confuse rather than clarify.

C. "includes a first mask memory location"[14]

USEI's Position	Defendants' Position
plain and ordinary meaning; alternatively: "includes a memory location for storing the first mask"	"includes a mask register for storing the first mask" [15]

Beginning with the Summary of Invention, the "present invention" is described as an apparatus comprising an "[i]ndication mask logic [that] selectively disables individual indication

[13] *See*, Ex. A-3, '874 Patent, Abstract ("Indication and interrupt signals generated by a network adapter representing asynchronous events are managed by a host system."); 3:1 ("indication values representing asynchronous events"), 3:7–9 ("an interrupt value representing indications of asynchronous events"), 36:50–52 ("These memory locations contain indications and interrupt values representing network adapter asynchronous events."); *see also*, 2:40–42, 2:56–57, and 5:39–44.

[14] This phrase appears in Claim 6 of the '874 Patent.

[15] Defendants have amended their proposed construction to the narrow the dispute between the parties on this term.

signals responsive to a write by the host processor to an indication ***register*** mask." Ex. A-3, '874 Patent, 2:63–66 (emphasis added). By the inventors' own characterization of the invention, the memory location to which a host writes mask values is a register. *See Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1330 (Fed. Cir. 2009) (the use of phrase "present invention" indicates the patentee's intent to limit the invention to that description).

The remainder of the written description reiterates that a mask memory location is a register. To be clear, there are other types of memory disclosed in the specification.[16] However, whenever a "*mask memory location"* is discussed, the invention exclusively employs registers.[17] No other type of "mask memory location" is disclosed in the specification or the prosecution history, and every embodiment of the invention relies on registers as mask memory locations.[18] The specification therefore equates a "mask memory location" to a mask register.[19] *See Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1305 (Fed. Cir. 2011) (a limiting construction "is required to tether the claims to what the specifications indicate the inventor actually invented."); *St. Clair Intellectual Prop. Consultants, Inc. v. Canon Inc.*, 412 F. App'x 270, 278 (Fed. Cir. 2011) (limiting "data formats" to still images based on the repeated

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[16] *See, e.g.*, Ex. A-3, '874 Patent, 5:55–57 (mentioning random access memory, BIOS ROM, and INFO EEPROM).

[17] *See, e.g.*, *id*. at 29:54–30:8 (defining "INDICATION MASK as a 6 bit register"); Fig. 17 (showing Indication Mask Register as a 6 bit register); 4:3–4; 34:12–44 (discussing how each bit of the Indication Mask Register is used to determine masking of a corresponding event); Fig. 23.

[18] *See id*. at 29:60–64 ("In the present embodiment, only Bits 6 through 1 are implemented in this register, while a ***register*** using a single bit or n bits may be used in ***other embodiments*** to mask a single or n indication sources."). The manner in which data is written to and erased from the *mask memory location* also requires the term be construed as a register. For example, unlike with other types of memory discussed in the patent, registers specifically require strobe and reset signals for data manipulation. *Id.* Fig. 17; 32:45–48; 32:54–55. These descriptions indicate that the patentees contemplated the use of registers alone for mask memory locations.

[19] Further, the prior art discussed in the patent employs registers as memory mask locations. *Id.* at 1:56–57 ("Prior art network adapters disable interrupts by using a ***mask register*** to mask interrupts.") (emphasis added). Given that the alleged problem solved by the '874 Patent invention is unrelated to the actual structure of the "mask memory location," *id*. at 2:4–10, the patent presumably adopts the meaning of the term from the prior art. *See Kumar v. Ovonic Battery Co.*, 351 F.3d 1364, 1368 (Fed. Cir. 2003) (stating that cited prior art "may indicate not only the meaning of the term to persons skilled in the art, but also that the patentee intended to adopt that meaning.").

use of "still" and "image" throughout the specification). Accordingly, Defendants' proposed construction is wholly consisted with the intrinsic evidence.

USEI's proposed construction, however, is divorced from these clear descriptions in the specification and merely rearranges words, adding nothing meaningful to the disputed phrase. For support, USEI points to portions of the specification that simply recite the term itself. *See, e.g.*, Ex. A-3, '874 Patent, 5:20–21 ("Interrupt and indication logic 10 includes mask memory locations 10a-c which contain the mask values").

Further, USEI's reliance on "memory cells" recited in Claim 15 is misplaced. USEI attempts to incorrectly read "cells" as a type of memory other than a register. "Cells," however, merely refers to portions or bits of a register. *Id.*, Claim 18 ("wherein the first *register comprises* a plurality of *memory cells*") (emphasis added). Moreover, the specification explains that, in "the present invention," the counter memory location, recited in Claim 15, is in fact "a *register* containing a counter value." *Id*. at 3:12–13 (emphasis added). Claim 15, therefore, does not suggest that a different memory structure is contemplated as a mask memory location.

D. "control means, coupled with the network interface means, for posting status information for use by the host system as feedback for optimizing the threshold value"[20]

USEI's Position	Defendants' Position
Function: Posting status information for use by the host system as feedback for optimizing the threshold value	Function: Automatically changing the threshold value, in response to status information, at the instruction of the host system, to make it as perfect, effective or functional as possible.
Structure: **XMIT Failure Register** (*see, e.g.*, Fig. 9 ("XMIT REGS."); Col. 16:9–23; Col. 4:56–60; Col. 14:53–57; Col. 19:13–35; Col. 28:67–29:2); and equivalents thereof.	Structure: '872 Patent, Figure 18, the aggregate of CRC logic 405, exclusive OR gate 407, transmit control logic 411, and underrun detector 413 and the connections by which they communicate.

[20] This limitation appears in Claim 10 of the '872 Patent.

USEI's proposed construction of the claimed function simply replicates the claim language itself, and fails to provide meaningful guidance to the jury on the disputed claim, which is not commonly understood by a lay person. By contrast, Defendants' proposed construction (1) provides meaningful guidance to an otherwise technical claim phrase and (2) gives effect to each feature the claim limitation. *See Multiform*, 133 F.3d at 1476 (when the term at issue is a term of art, rather than a common English word, claim construction is highly appropriate.). Defendants' proposed construction specifies that the threshold value is changed in response to status information to make the value as perfect, effective, or functional as possible. In prior litigation, the Northern District of California held that "optimize" means, within the context of the '872 Patent, changing the threshold value to "make it as perfect, effective, or functional as possible." *See* Ex. A-23, Dkt. 209, *3Com Corp. v. D-Link Systems, Inc.*, No. C-05-0098-VRW, at 10–12 (N.D. Cal. Jan. 26, 2007).

With regard to corresponding structure, Defendants correctly point to the aggregate of CRC logic 405, exclusive OR gate 407, transmit control logic 411, and underrun detector 413, as the structure that provides the claimed functions.[21] This structure is illustrated at FIG. 18, which is described as part of the "transmit logic 39." Ex. A-1, '872 Patent, 28:25–28. This logic operates to (1) detect when the rate at which the host interface transfers data "falls behind" the rate at which the transmit DMA logic transfers data on the data path (*i.e.*, occurrence of an underrun condition), and (2) generate a "bad frame signal" to the host interface that is used for posting status information of the underrun condition. *Id.*, 28:48–29:3. The threshold value is optimized by raising its value to avoid further underrun conditions. *Id.*, 29:48–51.

[21] USEI cites '872 Patent 4:56–60 to support its position (Plf. Br. at 9), but that citation actually supports Defendants' identification of corresponding structure. It clarifies that the claimed control means resides in transmit logic 39, which is where the CRC logic 405, exclusive OR gate 407, transmit logic 411, and underrun detector 413 identified by Defendants are located.

According to a described embodiment, underrun detector 413 generates the bad frame signal upon detecting that a transmit write signal (TXWR) is not present when expected, and transmits the bad frame signal to exclusive OR gate 407 and transmit control logic 411. *Id.* FIG. 18; 28:58–67. Exclusive OR gate 407 and transmit control logic 411 coordinate transmission of the bad frame signal, which is used to post status information of an underrun condition. In response to an indication of the underrun condition, the host raises the threshold value to avoid or minimize subsequent underrun conditions – avoiding the transmission of partial frames with bad CRC data. *Id.* 29:39–50. According to the described embodiment, the host does so by increasing the value of the XMIT START THRESH register:

> The adapter generates an indication of an underrun condition which is made available to the host through the XMIT FAILURE register. If such an underrun indication occurs, then the host driver should increase the value on the XMIT START THRESH 50 register. Further underrun indications should cause the driver to continually increase the XMIT START THRESH value.

Id., 29:46–53. This logic effectuates an "automatic" change in the threshold value where underrun detector 413 generates the bad frame signal and exclusive OR gate 407 and transmit control logic 411 transmit the underrun condition on line 409, at the instruction of the host, independent of other functionality. *See id.*, 28:25–29:2. The specification therefore makes it clear that each of the structures included in Defendants' proposed construction is necessary to perform the recited functions.

USEI points only to the XMIT FAILURE register as the corresponding structure. Plf. Br. at 9. However, as known in the art, a "register" does not "control" anything. The XMIT FAILURE register is simply a conduit used by transmit control logic 411 to effectuate the change in the threshold value. For example, "the adapter ***generates*** an indication of an underrun condition which is made available . . . ***through*** XMIT FAILURE register." Ex. A-1, '872 Patent,

29:46–48 (emphasis added). The bad frame signal asserted by transmit control logic 411 on line 409 is used to post status information ***through*** the XMIT FAILURE register. As such, the XMIT FAILURE register performs no function to change the threshold value, but instead is simply a conduit for other components that do so. *Asyst Tech., Inc. v. Empak, Inc.*, 268 F.3d 1364, 1371 (Fed. Cir. 2001) ("The corresponding structure to a function set forth in a means-plus-function limitation must actually perform the recited function, not merely enable the pertinent structure to operate as intended.").

Consistent with the foregoing, the XMIT FAILURE register performs a single function: returning the cause of failure of the attempt(s) to transmit a queued frame. If there is no error to report, each bit in the register has a value of zero. If there is an error to report, one or more bits have a non-zero value. Ex. A-1, '872 Patent, 19:16–34. Therefore, at most, the XMIT FAILURE register relied upon by USEI merely provides an indication of error in transmission. However, this does not perform the recited function, and thus cannot constitute the corresponding structure under 35 U.S.C. § 112(6).

USEI's citation to col. 4:56–60 of the '872 Patent supports Defendants' identification of corresponding structure. That citation clarifies that the claimed control means resides in transmit logic 39, which is where the logic 405, exclusive OR gate 407, transmit control logic 411, and underrun detector 413 identified by Defendants are located. Ex. A-1, '872 Patent, 28:40.

E. "means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame prior to transfer of all the data of the frame to the buffer memory from the host computer"[22]

USEI's Position	Defendants' Position
Function: initiating transmission of the frame prior to transfer of all the data of the frame to	Function: beginning transmission of the frame, as soon as the threshold condition is satisfied, subject to the risk of a collision, and

[22] This limitation appears in Claims 1 and 10 of the '872 Patent.

USEI's Position	Defendants' Position
the buffer memory from the host computer	before transfer of all the data of the frame to the buffer memory of the host computer.
Structure: 1. Transmit Start signal (See, e.g., Fig. 2, 38; Col. 4:35-45; 4:67-5:3; Fig. 12, xmitDataAvailable signal; Col. 24:60-25-2); and equivalents thereto.	Structure: INIT2 state 370 IMMEDIATE_THRESH_MET state 371 DOWNLOAD_THRESH_MET state 372 FRAME_RESIDENT state 373 Transmit DMA module 67 Ethernet Transmitter module 66 Transceiver 20 Data available control block 323.

1. Function.

The parties' dispute over the function centers on two distinct issues: first, whether "initiating transmission" means to *actually begin transmission*, or only refers to sending an *instruction* to begin transmission, and, second, whether prosecution history disclaimer applies to further limit the meaning of functional language to initiating transmission "as soon as the threshold condition is satisfied" and "subject to the risk of a collision."

As to the first point, the specification and prosecution history support Defendants' proposal. "When the [data downloaded to the adapter] meets the threshold, then ***actual transmission*** of the frame is initiated." Ex. A-1, '872 Patent, 2:52–53 (emphasis added). This passage states that "actual transmission"– that is, transmission on the network – is initiated when the threshold is met. The specification also states repeatedly that the transmit logic 39 and its subcomponents,[23] which are the structures that perform actual transmission,[24] are what "initiate transmission." Ex. A-1, '872 Patent, 5:2–3, 4:40–45, 9:5–7, 23:5–10.

The prosecution history also supports this view. The inventors described this means-

[23] Transmit DMA Module 67, Ethernet Transmitter Module (MAC) 66, and Transceiver 20.

[24] *See* Ex. A-1, '872 Patent, 4:3–7, 4:34–45, 9:13–51, 11:61–63. *See also* Ex. A-11, The Computer Glossary (6th ed. 1993) (defining "transceiver" as "Transmitter and receiver of analog or digital signals that comes in many forms"); Ex. A-12, Microsoft Press Computer Dictionary (2d ed. 1994) (defining "transceiver" as "A device that can both transmit and receive signals").

plus-function element as requiring *actual transmission* on the network. In describing how each limitation of Claim 1 of the '872 Patent was purportedly met by a system that they had built, the inventors explained that, in their system, "the transmission of data onto the local area network is overlapped with the receiving of data from the host," thus meeting "the fourth and final element of claim 1, a means for initiating transmission of a frame prior to transfer of all the data of the frame to the buffer." Ex. A-7, '872 file history, Decl. of March 2, 1994 at p. 2. Thus, the inventors clearly stated that the function called out in this claim element is met when the corresponding structure ***actually begins*** transmission.

The Examiner of the '872 and '094 Patents also understood "initiating transmission" to mean ***actual transmission*** on to the network, which is evidenced by statements made at three different points in prosecution.[25] An Examiner's understanding of a term is evidence of the understanding to one having skill in the art. *Salazar v. Procter & Gamble Co.*, 414 F.3d 1342, 1347 (Fed. Cir. 2005). Applicants never traversed or corrected Examiner's understanding.

Further, the testimony of USEI's expert, Dr. Mitzenmacher, in prior litigation supports Defendants' construction as well. Specifically, he has equated "initiat[ing] the transmission" with "***putting the front of the packet onto the network***." Ex. A-9, Trial Tr. at 156:3–8, 3Com Litigation (N.D. Cal. May 9, 2003) (emphasis added).

As to the second point, through an unambiguous disclaimer in the prosecution history of the '872 Patent, Applicants limited the scope of their alleged invention to initiating transmission "as soon as the threshold condition is satisfied" and "subject to the risk of a collision." *See*

[25] First, the Examiner rejected the "means . . . for initiating transmission" claim element as met by a prior art reference disclosing actually "*[t]ransmitting [a] frame* . . . in the manner described." Ex. A-19, '872 Pros. Hist., Oct. 26, 1993, Office Action at p. 3. Second, the Examiner made a double patenting rejection of an "initiating transmission" claim element based on a prior claim's *MAC* and *transmit DMA module* (which perform actual transmission and are included in Defendants' structure). Ex. A-20, '997 Application [continuation of the '872 Patent and parent of the '094 Patent], March 19, 1996, Office Action at p. 3. Third, the Examiner rejected another "initiating transmission" claim element as met by a prior art reference disclosing "*unloading [a] buffer to the network*" (*i.e.*, actual transmission). *Id.* at p. 7.

Computer Docking Station Corp. v. Dell, Inc., 519 F.3d 1366, 1374 (Fed. Cir. 2008) ("[A] patentee may limit the meaning of a claim term by making a clear and unmistakable disavowal of scope during prosecution."). In an amendment dated February 23, 1994, the Applicants added new claims, which addressed "a clear feature by which the present invention distinguishes over Firoozmand[]"and made their invention "fundamentally different." A-21, '872 Amend. at p. 4. They stated: "In the [prior art token ring] environment, no transmissions are initiated until the transmitting station receives the token from the network. . . . Accordingly, the Firoozmand[] reference does not initiate transmission to the network upon the threshold determination." *Id.* at p. 4–5. Moreover, the Applicants characterized the Firoozmand prior art as "***substantially different***" from the CSMA / CD network of their invention, "which begins transmission to the medium access controller as soon as the threshold determination is met for an incoming frame." *Id.* at p. 5.

By repeatedly contrasting Firoozmand, based on their view that it "does not initiate transmission to the network upon a threshold determination," the Applicants characterized the meaning of the relevant function here. Namely, the network adapter "begins transmission . . . **as soon as the threshold determination is met**[.]" *Id.* Moreover, the Applicants contrasted their invention over the prior art by saying it "**may suffer collisions**" and hence "initiates transmission without being assured . . . access to the communications medium," which they claimed made it a "much more sophisticated control environment" than Firoozmand. *Id.*[26] USEI's proposal acknowledges none of the limitations Applicants relied on to obtain allowance over the prior art. Federal Circuit case law is clear – USEI cannot undo the Applicants' prior disavowal in this

[26] Applicants' reference to CSMA / CD requires the possibility of collisions. "CD" stands for collision detection.

litigation. *See Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1372 (Fed. Cir. 2003).[27]

2. Structure.

The corresponding structure must meet two separate requirements: first, it has to be clearly linked to the claimed function, and, second, it must be "responsive to the threshold determination." As to the first requirement, the specification clearly and expressly links the transmit logic 39 and its subcomponents, Transmit DMA Module 67, Ethernet Transmitter Module (MAC) 66, and Transceiver 20,[28] to the function of "initiating transmission" by its very language. These are included among the corresponding structures set forth in Defendants' proposed construction.

- "The network interface controller includes *logic* for **initiating transmission** of the frame when the threshold [is reached.]" Ex. A-1, '872 Patent, Abstract, 2:22–27.[29]
- "[T]ransmit logic 39 is instructed to **begin transmission** of the frame." *Id.* at 5:2–3.
- "[T]hreshold store 43 . . . indicates an amount of data of a frame that must be resident in the frame buffer 34 before **transmission** of that frame may be **initiated** *by the transmit DMA logic and MAC 39*." *Id.* at 4:40–45 (also, reference number 39 refers to the transmit logic, *see id.* at 5:2–7, Fig. 2).
- "Also, the download DMA module 58 informs the *transmit DMA module 67* when it is time to **begin transmission**." *Id.* at 9:5–7.
- "[T]he transmit logic is waiting for the download operation on a third descriptor to either complete, or download sufficient data that the *transmit logic* may **begin transmission**." *Id.* at 23:5–10.

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[27] Further, USEI should be estopped from arguing that "initiating transmission of the frame" requires less than "beginning transmission of the frame, as soon as the threshold condition is satisfied, subject to the risk of a collision" by the doctrine of judicial estoppel. As explained by the Supreme Court, "where a party assumes a certain position in a legal proceeding, and succeeds in maintaining that position, he may not thereafter, simply because his interests have changed, assume a contrary position[.]" *New Hampshire v. Maine*, 532 U.S. 742, 743 (2001). USEI's predecessor in interest, 3Com, prevailed in a previous litigation on validity by asserting that the present limitation requires what Defendants propose. Ex. A-9, Tr. Test. at 156:3–8, 1374:5–14, 1403:2–5, 1406:6–10, 1406:14–18, *3Com Litigation* (N.D. Cal. May 9, 2003). USEI now asserts a position that is clearly inconsistent and imposes an unfair detriment on the Defendants by asserting a different meaning from the meaning publicly asserted by the patentee at trial. This form of judicial estoppel, *i.e.,* positions relating to claim meaning by a prevailing party, like those that give rise to prosecution history estoppel and run with the patent, should bind USEI.

[28] Ex. A-1, '872 Patent, 4:34–45, 5:3–5, Figs. 2, 5.

[29] This passage from the Abstract and Summary of the Invention sections indicates that the corresponding structure is "logic," not a signal as USEI suggests.

This linking is not surprising, given that these are the structures that perform actual transmission,[30] which as discussed above, is precisely what is required by the claimed function. *See supra* Section II.E.1.

USEI invokes the claim differentiation doctrine in arguing that the transmit logic structures that perform transmission cannot be corresponding structure because other claim limitations cover actual transmission, but this runs contrary to Federal Circuit precedent. The rule that a means-plus-function element must be construed according to the structures clearly linked to the function by the specification is a statutory **mandate**, whereas the rule against redundant claim language is only a **guideline**. *Nomos Corp. v. Brainlab USA, Inc.*, 357 F.3d 1364, 1368–69 (Fed. Cir. 2004) ("claim differentiation, which is a 'guide, not a rigid rule,' does not override the requirements of § 112, ¶ 6 when the 'claim will bear only one interpretation.'").

Defendants' proposal also includes additional structure, namely the Data Available Control Block 323 and its four states.[31] The inclusion of this is necessary in order to make the aggregate corresponding structure responsive to the threshold determination of the "means for monitoring." The parties agree that the "means for monitoring" corresponds to the counter, threshold store, and comparator,[32] and not the Threshold Logic 36 as USEI now argues in its brief. Plf. Br. at 13.

In the below figure, the "means for monitoring" corresponds to reference numerals 320 and 321 (in red). Its threshold determination is shown with the arrow from box labeled 321 to the box labeled 323 (in blue). The Data Available Control Block 323 and its four states are

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[30] *See* i*d.* at 4:3–7, 4:34–45, 9:13–51, 11:61–63.

[31] INIT2 state 370, IMMEDIATE_THRESH_MET state 371, DOWNLOAD_THRESH_MET state 372, and FRAME_RESIDENT state 373.

[32] *See* Ex. A-14, Pl. 4-3 Exh. A at 3. The agreed construction of "means for monitoring" is identical to the construction by Judge Ware in the parallel Northern District of California case. A-24, Dkt. 634 at p. 13, *U.S. Ethernet Innovations, LLC v. Acer, Inc., et al.*, Civ. A. No. 3:10-cv-03724 (N.D. Cal. August 29, 2012).

responsive to the threshold determination. Ex. A-1, '872 Patent, 24:67–25:2, 25:7–18, 27:53–28:23, Fig. 12, Fig. 17 (showing state changes on threshold determination).

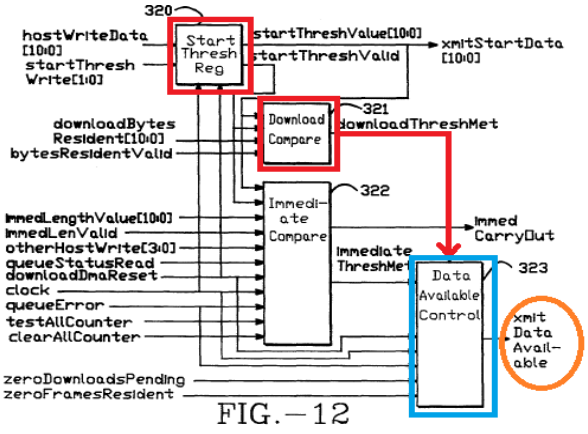

FIG.—12

(*Id.* at Fig. 12.)

The four states included in Defendants' proposal are a necessary part of the corresponding structure: they pertain to an initial condition when no threshold determination is made, and three conditions under which the Data Available Control 323 notifies the transmit logic that data is available to transmit. *Id.* at 25:7–18; 27:58–59; 28:11–14; 27:65–28:3. USEI's argument that including the states of the Data Available Control would exclude the preferred embodiment is incorrect. *See* Plf. Br. at 15. The "Overview" section relied on by USEI summarizes the sole enabling embodiment, which actually includes Defendants' proposed structure – the Data Available Control Block 323 and its four states. *See* Ex. A-1, '872 Patent, 3:58; 23:20–27.

USEI's identified structure, the Transmit Start Signal, does not perform the claimed function of "initiating transmission." USEI admits that, "This signal—referred to as 'Transmit Start' **instructs the transmit logic to 'initiate transmission,'** as recited by the claimed function." Plf. Brief at 13 (emphasis added). USEI has also noted that "[w]hen the threshold amount of data is resident in the buffer . . . transmit logic 39 **is instructed to begin transmission** of the frame." *Id.* (emphasis in original) (citing '872 Patent at 4:67–5:3). Thus, USEI concedes

that it is the *transmit logic* that initiates transmission, not the Transmit Start Signal. *Asyst Techs., Inc*, 268 F.3d at 1371 ("The corresponding structure to a function set forth in a means-plus-function limitation must actually perform the recited function, not merely enable the pertinent structure to operate as intended."). At best, as USEI acknowledged, it performs the unclaimed function of "instructing other structures to initiate transmission," not the function called out in this claim element.

Moreover, USEI ignores the numerous structures in the specification (noted above) that are clearly and expressly linked in the specification and file history to "initiating transmission." Finally, there is nothing in the specification or prosecution history, nor has USEI cited anything, to clearly link the Transmit Start Signal to "initiating transmission," so it cannot be corresponding structure.

F. "interrupt means, coupled to the second memory location and responsive to the interrupt value from said second memory location, for generating the interrupt signal to the host"[33]

USEI's Position	Defendants' Position
Function: generating the interrupt signal to the host	Function: To use an interrupt value as an input to generate an interrupt signal as an output to the host.
Structure: Interrupt Controller (*See, e.g.*, Fig. 4, 60; Col. 7:55-63); and equivalents thereto.	Structure: Indefinite because one of ordinary skill in the art would not know what structure is linked to "interrupt means." Or, in the alternative, in the event that this term is not found indefinite, and without conceding that the specification contains sufficient structure: OR gate 303 having inputs that are connected directly to each output of the second memory location; AND gate 305 having an input that is connected directly to the output of the OR gate 303; multiplexer 306 having an input that is connected directly to the output of the AND gate 305; and multiplexer 304 having an input that is directly connected to an output of the multiplexer 306

[33] This limitation appears in Claim 1 of the '874 Patent.

1. The Lack of Corresponding Structure Renders this Claim Term Indefinite.

The "interrupt means…" limitation is indefinite because the patent does not disclose any structure that is ***clearly linked or associated with*** the claimed function. *See Ergo Licensing, LLC v. CareFusion 303, Inc.*, 673 F.3d 1361, 1363 (Fed. Cir. 2012) ("Such structure must be clearly linked or associated with the claimed function . . . . Although [§ 112 ¶ 6] statutorily provides that one may use means-plus-function language in a claim, one is still subject to the requirement that a claim ***particularly point out and distinctly claim*** the invention.") (internal citations and quotations omitted; emphasis added).

With respect to function, USEI does not dispute the accuracy of Defendants' proposal, but simply argues that Defendants' proposed function adds "unnecessary limitations" that are already made clear by the claim language. *See* Plf. Br. at 16. But it is black letter law that "[t]he court must construe the function of a means-plus-function limitation to include the limitations contained in the claim language . . . ." *In re Aoyama*, 656 F.3d 1293, 1296 (Fed. Cir. 2011) (internal quotations omitted). Defendants' proposed function does precisely that – it includes the limitations contained in the claim language, as USEI concedes. In contrast, USEI's proposed function improperly ignores the "coupled to the second memory location and responsive to the interrupt value from said memory location" limitation.

The specification, however, fails to disclose any structure that is clearly linked to the claimed function. The only disclosure that might even arguably relate to the use of an interrupt value as an input to generate an interrupt signal to the host is that shown in Figures 24 and 25, collectively. Figure 24 purports to be "a schematic illustrating when an interrupt signal should be generated," while Figure 25 purports to be "a schematic illustrating the generation of interrupt level signals." Ex. A-3, '874 Patent at 4:20–23.

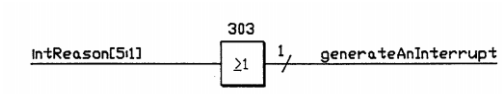

FIG.–24

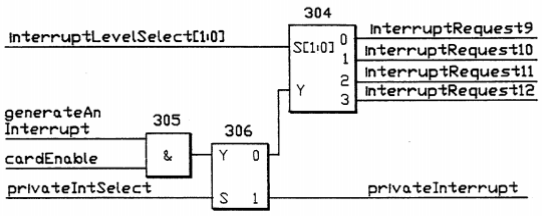

FIG.–25

Figures 24 and 25 together depict the following specific structure: an OR gate (303, Fig. 24), an AND gate (305, Fig. 25), and two multiplexers (304 and 306, Fig. 25). "IntReason[5:1]" presumably refers to any signal coming from the second memory location (depicted in Fig. 12 as "IntReason 210"). *Id.* at 34:45–49; *see also id.*, Fig. 12. Figure 24 shows that when OR gate 303 receives such a signal from the second memory location, it asserts a "generateAnInterrupt" signal, *id.* at 34:45–49, shown as an input in Figure 25 to AND gate 305. If it also receives a "cardEnable" signal (also shown in Figure 25), AND gate 305 passes on the "generateAnInterrupt" signal to multiplexer 306. *Id.* at 34:51–56. Unless it receives a "privateIntSelect" signal, multiplexer 306 then routes the "generateAnInterrupt" signal to multiplexer 304. *Id.* at 34:56–62. Finally, the multiplexor 304 routes the "generateAnInterrupt" signal to one of its four outputs: "interruptRequest9," "interruptRequest10," "interruptRequest11," and "interruptRequest12." But it is unclear from Figure 25 whether the signal is then passed on (as required by Claim 1) and, if so, where it is routed to. Thus, the specification does not clearly link or associate the structure of Figures 24 and 25 with the claimed function of the "interrupt means . . ." limitation.

Even if the Court were to conclude that the patent does demonstrate the requisite linkage between claimed function and associated structure, the only disclosed structure that could

conceivably be associated with using an interrupt value as an input to generate an interrupt signal as an output to the host is that shown in Figures 24 and 25. Defendants' alternative construction accordingly consists of the structure of Figures 24 and 25 (namely, OR gate 303, AND gate 305, and multiplexers 304 and 306).

2. USEI's Proposed Structure Is Inconsistent with the Claim Language and Specification.

USEI incorrectly asserts that the corresponding structure is the Interrupt Controller Module 60 shown in Figure 4 of the '874 Patent. USEI's contention rests entirely on the following sentence from the specification: "The interrupt controller module 60 then passes the interrupt signals through various enables and masks before ORing them together and driving the result onto the host bus." Ex. A-3, '874 Patent at 7:60–63. But rather than provide the needed clear linkage between Interrupt Controller Module 60 and the "interrupt means…" limitation, that sentence simply refers vaguely to "various enables and masks" and to an equally vague "ORing" process. It does not identify the precise structure associated with the "various enables and masks[,]" nor does it specify what specific structure is carrying out the referenced "ORing."

USEI's proposed structure also ignores the "coupled to the second memory location and responsive to the interrupt value from said second memory location" language of this limitation, creating at least two problems. First, per Claim 1 the "interrupt means" must be "***coupled to*** the second memory location." *Id.* at Claim 1 (emphasis added). The plain and ordinary meaning of "couple" is to link two separate structures. *See, e.g.*, A-22, IEEE Standard Dictionary of Electrical and Electronics Terms 215 (4th ed. 1988) ("coupling . . . (3) (data transmission). The association of two or more circuits or systems in such a way that power or signal information may be transferred from one to another."). Thus, the claim requires that the structure for the "interrupt means" be linked to a separate structure – the second memory location. But the

second memory location, which is depicted as either "IntReason 210" or "OtherInt 209" in Figure 12, resides ***within*** Interrupt Controller Module 60.[34] *See, e.g.*, Ex. A-3, '874 Patent at 27:1–8 ("In one embodiment of the present invention, the following registers are resident in the Interrupt Controller Module 60 of FIG. 4 . . . . INT REASON"); *id.* at 7:56-58. Interrupt Controller Module 60, therefore, cannot as a whole be the structure for "interrupt means" because it cannot be coupled to itself.

Second, Claim 1 also requires that the "interrupt means" be "***responsive to*** the interrupt value from said second memory location." *Id.* at Claim 1 (emphasis added). Again, since the second memory location (depicted as "IntReason 210" or "OtherInt 209" in Figure 12) resides **within** Interrupt Controller Module 60, Interrupt Controller Module 60 cannot be the structure for "interrupt means" because it cannot be responsive to a value generated internally by one of its own subcomponents. Thus, the entirety of Interrupt Controller Module 60 cannot be the structure associated with "interrupt means . . . ."

G. "means for comparing the counter to the threshold value in the alterable storage location and generating an indication signal to the host processor responsive to a comparison of the counter and the alterable storage location"[35]

USEI's Position	Defendants' Position
Function identified by both USEI and Defendants: (1) comparing the value generated by the counter to the threshold value in the alterable storage location; and (2) generating an indication signal to the host processor responsive to a comparison of the value generated by the counter and the value in the alterable storage location.	
Structure:	Structure:

[34] The specification further makes clear that Interrupt Controller Module 60 contains not only the second memory location, but also the first mask logic, first memory location, and second mask logic elements (as shown in Figure 12 of the patent) that precede the "interrupt means…" limitation of Claim 1. *See* Ex. A-3, '874 Patent at 27:1–31:29 ("In one embodiment of the present invention, the following registers are resident in the Interrupt Controller Module 60 of FIG. 4 . . . . FIG. 12 illustrates the relationship between the above registers.").

[35] This claim limitation appears in Claim 1 of the '459 Patent.

1. **comparator** (*See, e.g.*, Fig. 14, 213; Col. 32:23-30; Fig. 14, 224; Col. 32:44-50; Fig. 21, 318; Col. 36:6-16; Fig. 23, 341; Col. 37:58-59; Fig. 24, 511; Fig. 26, 517, Col 39: 1-5; Fig. 31, 615; Col. 40:41-53); and equivalents thereto. 2. **control block** (*See, e.g.*, Fig. 14, 210; Col. 31:41-49; Fig. 14, 225; Col. 32:31- 36; Fig. 4; Col. 34:33-38; Fig. 24, 512; Fig. 27, 512; Col. 38:51-55; Fig. 33, 625; Col. 41:1-18); and equivalents thereto.	Indefinite because one of ordinary skill in the art cannot discern a single structure performing both "comparing the counter to the threshold value" and "generating an indication signal to the host processor," as required by claim 1, and 2) because the "comparing" structures are purely functional blocks, lacking structure by which equivalents can be discerned to determine claim scope. Alternatively, in the event that this term is not found indefinite, and without conceding that the specification contains sufficient structure: 1. Corresponding structure for "comparing the counter to the threshold value" is comparator 224, as illustrated in FIG.14. 2. Corresponding structure for "generating an indication signal to the host processor" is the "Early Rcv Control 225" in FIG. 14 (having the features of Fig. 18) combined with the host bus interface 51 as illustrated in FIG. 4 and the host bus.

This limitation from Claim 1 of the '459 Patent was construed by the *Acer* Court to be arguably indefinite. *See* A-24, Dkt. 634, *Acer Litigation*, Second Claim Construction Order, at p. 8–11. In light of that Order, and as addressed in Defendants' Motion for Summary Judgment of Invalidity based on Indefiniteness for the '459 and '313 Patent (Dkt. No 169, 6:12-cv-235), the "means for comparing" limitation is indefinite because the '459 Patent fails to disclose a single structure that is capable of performing both functions (comparing and generating an indication signal) recited in those claims, and nothing in the intrinsic evidence would lead a person of ordinary skill in the art to combine separate components to do so.

Alternatively, to the extent the Court does not find this term indefinite, the parties agree that this limitation should be interpreted as a means plus function under 35 U.S.C. §112, ¶6. *See* Plf. Br. at 19. The parties also agree on the two recited functions. The only dispute is the corresponding structure for performing those functions. Without conceding that the specification contains sufficient structure to support this limitation, Defendants identify the following structures.

To the extent one exists, the sole corresponding structure for the function of "comparing the counter to the threshold value" is the comparator 224 of Fig. 14 and its corresponding input and output signals. Comparator 224 compares signal RCV FRAME LENGTH [10:0][36] to threshold value LOOK AHEAD THRESH. Ex. A-4, '459 Patent at 32:47–50 (describing the comparison); 32:9–10 (identifying the threshold value).

None of the other "structures" identified by USEI performs the claimed comparing function, *i.e.*, comparing the claimed counter with a threshold value. The counter in Claim 1 is "for counting the amount of data transferred to or from the buffer memory." None of the other structures cited by USEI compare a threshold value against such a counter:

- **Fig. 14, 213**: Comparator 213 compares a frame length (input a) to a sum (input b) of lengthLeft threshold and a count of received data from the frame, the sum being output by counter 216. The counter 216 is initialized to, and starts counting up from, the lengthLeft threshold value, as indicated by input D of counter 226 receiving output Q of the lengthLeft ThreshReg 221. *See* Ex. A-4, '459 Patent, Fig. 14; 31:60–62; 32:15–17. Thus, neither input to comparator 213 is a count of an amount of data received in a buffer.
- **Fig. 21, 318**: Comparator 318 also compares a "sum [that] is . . . entered to the a input of comparator 318 with LOOK AHEAD THRESH [10.0] entered at the b input," not a count of an amount of data itself. *Id.* at 36:14–16.
- **Fig. 23, 341**: Comparator 341 also does not compare against the claimed count. The input bytesRemaining[10:0] to comparator 341 was cited by Judge Ware in a previous Markman ruling as explicitly not being an example of "the amount of data transferred." *See* A-24, Dkt. 634, *Acer Litigation*, Second Claim Construction Order at n.12; *see also id.* at 8–10 (citing '459 Patent, 37:59–38:8).
- **Fig. 24, 511**: Threshold compare block 511 of Fig. 24, like comparator 213 above, compares a frame length to a sum, not the claimed count itself. Ex. A-4, '459 Patent 38:26–32; 38:65–39:4, element 516 of Fig. 26.
- **Fig. 26, 517**: Comparator 517 is the comparator that performs the comparison of threshold compare block 511, distinguished above. *Id*. at 38:65–39:4; element 511 of Fig. 26.

[36] The '459 Patent does not explain the provenance of RCV FRAME LENGTH [10:0], and in particular, whether this signal is from a count of an amount of data transferred to or from a buffer memory, as recited by claim 1. But the Patent implies that this is the case (*id*. at 34:17–20), which is in contrast to inputs to other comparators identified by USEI and discussed below.

- **Fig. 31, 615**: Comparator 615, like elements 213, 511, and 517, compares a frame size against a sum of a threshold value and a transmitByteCnt value. *Id*. at element 614 of Fig. 31; 40:24–31.

Further, all of USEI's proposed "structures" are purely functional and therefore indefinite and insufficient.[37] Corresponding structure must be defined by more than mere reiteration of the function to which it corresponds. *Ergo Licensing*, 373 F.3d at 1365; *see also Noah Systems, Inc. v. Intuit Inc.*, 625 F.3d 1302, 1318 (Fed.Cir.2012); *Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1340–41 (Fed. Cir. 2008). Here, the comparators identified by USEI are merely reiteration of the comparing function. Ex. A-4, '459 Patent at 4:19–40 (describing USEI's "structure" as functional block diagrams). Simply labeling a functional block "comparator" does not disclose a structure by which the public can discern equivalents defining claim scope. For instance, the '459 disclosure does not indicate whether the cited comparators are analog or digital, and if digital, whether they receive compared multi-bit values in serial or parallel. Thus, USEI's proposed "structures" are insufficient to define equivalents for ascertaining claim scope.

For the second function, "generating an indication signal to the host processor responsive to a comparison . . .," Defendants identify as corresponding structure the combination of the "Early Rcv Control 225" of Fig. 14, having the features described with reference to Fig. 18, the host bus interface 51 of Fig. 4, and the host bus. In particular, Defendants contend that the corresponding structure must include the host bus interface 51 in Fig. 4 and the host bus so that the structure allows for the indication signal to have a path "to the host processor" as recited in Claim 1 of the '459 Patent. Without the host bus interface 51 and the host bus, no indication signal can be generated "to the host processor."

Each component identified by Defendants is necessary to perform the claimed function.

[37] Every independent claim of the '459 Patent recites a "means for comparing a counter to an [X] threshold." For the same reasons, USEI's comparators are also insufficient to establish corresponding structure for all asserted claims.

The Early Rcv Control 225 receives the lookaheadThreshMet signal from the comparator 224 and, in response, "asserts EARLY RCV." Ex. A-4, '459 Patent at 32:31–56; Fig. 18. This asserted signal is conveyed to the host via the host interface 51 and the host bus. *Id.* at 6:13–15; 5:68–6:2. Finally, features of Early Rcv Control block 225 are defined in Fig. 18. *Id*. at 34:8–23. In contrast, none of the structures identified by USEI for the comparing function perform the generating function because they 1) are not responsive to the output of the comparing function, and 2) lack any conduit to the host processor. *See* Plf. Br. at 19.

Moreover, the structures identified by USEI for the generating function do not perform all aspects of this function. The Rcv Complete Control block 210 of Fig. 14 is not "responsive to a comparison of the value generated by the counter" because, as explained above, comparator 213 does not compare against the counter recited by Claims 1 or 22. *See* A-4, '459 Patent, Fig. 14; 31:60–62; 32:15–17. And the Early Rcv Control 225, in isolation, cannot be a corresponding structure because it does not "generat[e] an indication signal to the host processor[;]" other circuitry, including the host bus, is required, as explained above. The EARLY INDICATION LATCH block 512 of Fig. 24 is based on "THRESHOLD COMPARE block 511[, which] is used to assert COMPLETE THRESH MET," and as such, cannot be "responsive to a comparison of the value generated by the counter" of the present claims for the reasons explained above for block 511. *See id.* at 38:42–43. The same reasoning applies to latch indication block 625 of Fig. 33, which is a component of block 512. *See id.* at 41:1–18.

USEI cites to Dr. Mitzenmacher's testimony, but he fails to address a key feature: the indication signal must be sent to the host processor. *See* Plf. Br., Decl. of Dr. Mitzenmacher at ¶¶ 13–17. To perform this function, the structure corresponding to the generating function must

include a signal path to the host, *i.e*, the host bus.[38]

H. "host interface means, sharing host address space including a prespecified block of host addresses of limited size defining a first area and a second area, and coupled with the buffer memory, for mapping data addressed to the first area into the transmit buffer, mapping data in the receive buffer into the second area, and uploading data from the receive buffer to the host"[39]

USEI's Position	Defendants' Position
Function identified by USEI and Defendants: (1) mapping data addressed to the first area into the transmit data buffer; (2) mapping data in the receive buffer into the second area; and (3) uploading data from the receive buffer to the host.	
Structure: 1. **XMIT AREA** (*See, e.g.*, Col. 10:46-54; Col. 17:25-36; Fig. 3; Fig. 9 (XMIT REGS); and equivalents thereto. 2. **XFER AREA** (*See, e.g.*, Col. 10:55-58; Col. 15:10-18; Col. 25:34-41; Fig. 3; Fig. 11 (XFER REGS); and equivalents thereto. 3. **upload DMA logic** (*See, e.g.*, Fig. 2, 57; Fig. 3; Fig. 11, 300; Col. 2:47-51; Col. 6:13- 18; Col. 8:65-9:12; Col. 9:60-10:2; Col. 23:14-19); and equivalents thereto.	Structure: No disclosure of a single structure capable of performing all three functions, and nothing in the intrinsic evidence that would lead a person of ordinary skill in the art to group these individual components into a single component.

As with the claim term in Section G *supra*, the *Acer* Court also construed this claim limitation and found it arguably invalid as indefinite. Defendants' arguments regarding the indefiniteness of this limitation are set forth in their Motion for Summary Judgment. As explained in that Motion, the present means-plus-function element is indefinite for lacking a corresponding structure because no reasonably related set of elements in the specification performs all three specifications. To the extent that the Court finds Claim 13 of the '313 Patent not indefinite, however, Defendants agree with USEI's identification of the three recited functions and the proposed corresponding structures: the XMIT AREA, the XFER AREA, and the upload DMA logic.

[38] Every independent claim of the '459 patent recites "generating an indication signal to the host." For the same reasons as set forth for Claim 1, Defendants maintain all pending claims require the host bus or an equivalent.

[39] This claim limitation appears in Claim 13 of the '313 Patent.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

Pursuant to the Federal Rules of Civil Procedure and the Local Rules, I hereby certify that all counsel of record who have appeared in this case are being served today with a copy of the foregoing via the Court's CM/ECF system.

Dated: March 11, 2013

/s/ *Steven G. Schortgen*
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